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NAVY ELECTRONICS LAB SAN DIEGO CALIF  
A PASSIVE SONAR SIGNAL PROCESSOR FOR EXPERIMENTAL USE.(U)  
AUG 65 M D FLASKA, W H LITTRELL  
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A PASSIVE SONAR SIGNAL PROCESSOR FOR EXPERIMENTAL USE.

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A PASSIVE SONAR SIGNAL PROCESSOR FOR  
EXPERIMENTAL USE (U)

by

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## INTRODUCTION

The purpose of this memorandum is to provide a functional description of a passive sonar signal processor (DELTIC Cross-Correlator and Frequency Analyzer) under development by Code 3150 and to describe briefly its intended use. The concept and basic design of this processor is attributable in large part to the efforts of William E. Klund. The information presented represents only preliminary effort in a program to develop computer-aided techniques for passive sonar detection. Distribution will be primarily limited to interested individuals within the laboratory.

## COMPUTER-AIDED DETECTION

In recent years, much progress has been made in developing techniques to apply general purpose digital computers in the area of active sonar detection.<sup>1,2,3</sup> Most new sonar system designs incorporate a computer to assist the operator in evaluating the enormous amount of information provided by long range active sonars having high resolution in range, bearing and doppler. It is generally presumed that such a computer will also relieve the operator requirements in other areas such as passive detection, classification, fire control, countermeasures, etc. While these are reasonable presumptions, the methods of implementing these functions are not nearly as well defined.

1. NEL Report 1060 "Lorad Status Report" of 9 Oct 1961 (CONF)
2. Proceedings of 8th Navy Science Symposium, U.S. Naval Postgraduate School, Monterey, California, 14 May 1964: "The General Purpose Computer for Sonar Signal Processing and Target Classification" by R. D. Isaak
3. NEL Technical Memorandum 747 "Computer-Aided Display for Lorad" of 16 Dec 1964 by V. D. Kuhlmann (CONF)

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Modern passive sonar systems for long range detection characteristically provide output signals on a multiplicity of preformed beams. These must be either observed simultaneously or at sampling intervals which retain all significant information. The problems associated with reducing this information to a form easily interpreted by an operator without degrading system performance are to be addressed through the use of the DELTIC Cross-Correlator and Frequency Analyzer described here. Some major factors which complicate the use of computers in the reduction and evaluation of this information are:

- ✓ a. Data rates are high, imposing severe computer memory and speed requirements.
- b. Passive detection normally involves integration over a long time interval.
- c. Optimum integration time cannot be pre-determined.
- d. Integration across bearing intervals of interest requires tracking from beam to beam, resulting in a large number of possible tracks to be investigated during the detection process.
- e. Spectral analysis of the signals is difficult to optimize. Operator evaluation of spectral information in the passive detection problem is largely subjective. ✓

A major consideration in developing computer techniques for passive detection will be the trade-offs between special purpose devices at the signal processor interface and data processing within the

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computer. It is anticipated that experiments using the DELTIC Cross-Correlator and Frequency Analyzer will assist in defining functions to be performed and in determining which should be performed external to the computer. The development program will ultimately include simultaneous processing for active and passive detection with a single computer in real time.

#### EXPERIMENTAL PASSIVE DETECTION SYSTEM

A functional representation of the experimental system is given in Figure 1.

##### Sensors

The sensor configuration consists of two linear arrays, each comprised of five (5) hydrophones with one-half wavelength spacing at 1500 cps, mounted on the forward wings of the USS BAYA. Either the unshaded array beams or a pair of single hydrophones may be selected to provide the signal inputs to the processor. Equalization is provided and filtering is selectable for either the 100 - 1200 cps and/or the 100 - 4800 cps band.

*should be lower*

##### Signal Processor

The DELTIC Cross-Correlator and Frequency Analyzer provides a continuous bearing scan in the forward thirty degree sector. The cross-correlator is a clipped, digital device designed to process signals in the zero to five kilocycle band with an azimuthal resolution of approximately one-half degree. The resolution actually achieved will depend upon the spectrum of the received signal.



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The inputs to the cross-correlator are the signals from two separated hydrophones or hydrophone arrays. By the use of DELTICS in each channel, the signals are time compressed and cross-correlated to provide a measure of the coherent signal power that exists within a  $30^{\circ}$  bearing aperture centered on the bow. The bearing aperture limits correspond to plus and minus 3.2 milliseconds relative signal delay in the two channels. This 6.4 millisecond delay window is divided into sixty-four equal increments of 100 microseconds, corresponding to bearing increments of approximately  $0.5^{\circ}$ , and a serial correlation is performed for each increment to scan the  $30^{\circ}$  sector. The output signal for each correlation is independently thresholded to normalize the azimuthal noise and then applied to a data rate limiter. If the threshold of the data rate limiter is exceeded, the digital representation of the DC correlation level and the corresponding true and relative bearing codes are formed in a buffer register at the AN/USQ-20 computer interface.

The frequency analysis is also a clipped process. It extracts spectral information in the 100 to 1250 cps band with an approximate resolution of one cps. The input signal is supplied by one of the arrays or hydrophones used with the cross-correlator. The signal is time compressed in a DELTIC and compared with the output of a digitally controlled VCO to perform a spectral analysis of the band once each .8192 seconds. Amplitude and frequency data are formed in a buffer register for each resolvable frequency interval. A threshold circuit compares the spectral amplitude with a threshold level supplied from the computer. The data which exceed the threshold are gated into the computer for computer analysis.



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#### Computer

The computer employed is the CP-642A (AN/USQ-20). Programs will be developed for real-time on-line processing of the data with maximum efficiency. Functions may be simulated which will ultimately be implemented with external special purpose devices.

#### Synthetic Display

Display formats will be developed for symbolically representing the processed data on a CRT display. The same display used for active sonar data will be employed. The display currently used for this purpose is a Tonotron storage display. It accepts data from the computer exclusively.

#### Monitor Display

To supplement the computer controlled synthetic display, a monitor CRT display will present either the correlation or frequency analysis information taken directly from the signal processor in selectable A-scan or B-scan format. This display will provide for equipment fault monitoring. It also is expected to provide a useful insight into data characteristics, under varying conditions, particularly during the initial phases of computer program development.

#### DETAILED DESCRIPTION OF THE DELTIC CROSS-CORRELATOR AND FREQUENCY ANALYZER

Reference to Figure 2 will supplement the following discussion of the DELTIC Cross-Correlator and Frequency Analyzer.

#### DELTIC Cross-Correlator

The signal in Channel A is infinitely clipped, sampled at a 10 KC rate by the S<sub>-32</sub> sample pulse, and inserted in a 2048 bit delay line

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that is driven at a 20.47 mc rate. Because the  $S_{-32}$  sample pulse is derived by a 2047 frequency division of the basic clock, the  $S_{-32}$  sample pulse occurs once per 20.47 basic clock pulses. Since this condition obtains in a delay line of 2048 bits, with appropriate gating the newest sample will be entered and the oldest sample deleted. The output of this delay line is sampled in the same fashion by an identical delay line with the same timing except that the  $S_0$  sample pulse for the second line is delayed in time with respect to the  $S_{-32}$  sample pulse by a 32 basic clock pulse. The output of the second delay line is the Channel A input to a modulo 2 adder.

The Channel B signal is infinitely clipped and processed in a 2048 bit delay line that operates in exactly the same mode as the second line of Channel A; that is, the  $S_0$  pulse is used to sample the clipped signal. The contents of this line are transferred as a single block of information into a 2047 bit line that is also operated at 20.47 mc. This transfer is accomplished every 6.4 milliseconds by a 100 microsecond gate pulse. This gate pulse is generated when a count of 32 exists in the six least significant bits of a 13-stage,  $S_0$  pulse counter that defines the relative bearing for each correlation cycle. The output of the second delay line is the Channel B input to the modulo 2 adder.

The output of the modulo 2 adder is sampled at a 20.47 mc rate and a count is accumulated in one of two gated counters over the period of the correlation cycle. The two counters are employed during alternate correlation cycles. A threshold from the threshold memory is preset into the counter that is inactive during one correlation cycle in

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preparation for the next cycle in which the counter will perform the integration function. The outputs of the counters are alternately gated for comparison with a preset number in the data rate limiter. If this number is exceeded, an input data request is sent to the computer and the output of the counter is stored in an output register. The six most significant bits of this stored output and the delayed six bit time delay code, i.e., relative bearing, are converted to analog voltages for the monitor display. The relative bearing code and a true bearing formed by parallel addition of a ten bit course code with a modified relative bearing code are periodically updated in the output data register. Of particular importance in understanding the generation of true bearing by a single parallel addition is the modification of the relative bearing code by the extension of the condition of the sixth bit to the four most significant bits, and the fact that the initiation of a new group of 64 correlation cycles occurs at the midpoint of the relative bearing count.

The twelve bit threshold values and the associated 6-bit relative bearing addresses are inserted in an input register under computer program control. The threshold memory unit is organized as a 256 word by 3-bit word memory. The input threshold word is multiplexed to sequentially store the original 12-bits in four adjacent words, and an output demultiplexer is sequentially scanned to accomplish the presetting of the integrating counters. The memory is addressed for readout by a relative bearing code.



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To summarize the operation, it is to be noted that because of the 32 clock pulse interval between the sample pulses  $S_0$  and  $S_{-32}$ , the bits in the second delay line of Channel A are delayed 3.2 milliseconds with respect to the time that the signal was sampled. If the signal arrival at Channel B is delayed with respect to that of Channel A by 3.2 milliseconds, then the sampled signals would correlate during the transfer period, i.e., the first correlation cycle of the 64-cycle group. For the other extreme, the arrival of the Channel A signal is delayed by 3.2 milliseconds with respect to the arrival of the Channel B signal. The signal transferred to the second delay line of Channel B will be stored with no change in signal composition until the 64th correlation cycle occurs, when the second line of Channel A will have acquired the correct group of samples. For smaller values of signal delay, the correlation will occur on intermediate cycles, and no correlation can be detected for values of signal delay in excess of 3.2 milliseconds. For each correlation cycle, i.e., relative bearing code, there exists an independent threshold level that is subject to automatic change as determined by on-line computer data analysis. This prevents excessive computer loading due to noise spikes. The program will determine thresholds as a function of relative bearings but will use true bearing data for target detection. Processed data will be appropriately formatted for symbolic display.

#### Frequency Analyzer

The same hydrophone array or hydrophone that supplies signal to Channel A is used as a signal input for Channel C, the frequency analysis channel.

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The signal of Channel C is clipped and sampled at a 2500 cps rate and inserted in a 2047 bit delay line that is clocked at a 20.47 megacycle rate. Every .8192 seconds the content of this line is gated into a second line that is operated in an invariant circulatory mode. The output of this second line provides one input to a non-return-to-zero modulo 2 adder.

The output of the thirteen bit counter that controls the basic timing pulses and gates is combined with feedback from the clipped voltage controlled oscillator to provide the control voltage for the VCO and a display sweep. The clipped VCO output is swept linearly in frequency from 20.49 mc to 10.25 mc every .8192 seconds and serves as the other input to the modulo 2 adder.

A 100 microsecond sample of the output of the modulo 2 adder is applied to a matched Gaussian filter every 800 microseconds. The peak detected filter output is applied as a display quantity, a comparator input, and is also converted to a twelve-bit digital number for transfer to the computer if the value has exceeded the comparator threshold. This analog threshold is derived from the conversion of a twelve bit number that is provided under computer control, with an optional manual control. If the threshold has been exceeded an indicator is illuminated, and a data request is generated to initiate transfer to the computer of the digital amplitude and the ten most significant bits of the thirteen stage counter which represent frequency.

The manual threshold switch and the pushbutton pulse generator provide a means to change the content of the threshold register manually,

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and to update this computer memory threshold by a transfer of the content of the threshold register to the data register and a generation of an external interrupt.

The sweep repetition rate pulse clears the amplitude bits of the data register and generates a data request to provide a timing marker to the computer every .8192 seconds.

The comparator indicator flip-flop causes an indicator light to illuminate if the threshold has been exceeded and is reset by the sweep repetition rate pulse. This function provides both an operational and a test monitor.

The feedback test switch provides a test and calibration capability for the conversion and comparison processes.

The dynamic test switch and manual test control allow the introduction of a 10.235 mc signal of a precise amplitude to calibrate the linearity of the detector and to provide an estimate of error which may be incurred in the clipping and multiplication process due to waveform asymmetry introduced by large temperature changes.



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FIGURES

	Figure No.
Experimental Passive Detection System	1.
Functional Block Diagram - Deltic Cross-Correlator and Frequency Analyzer	2.

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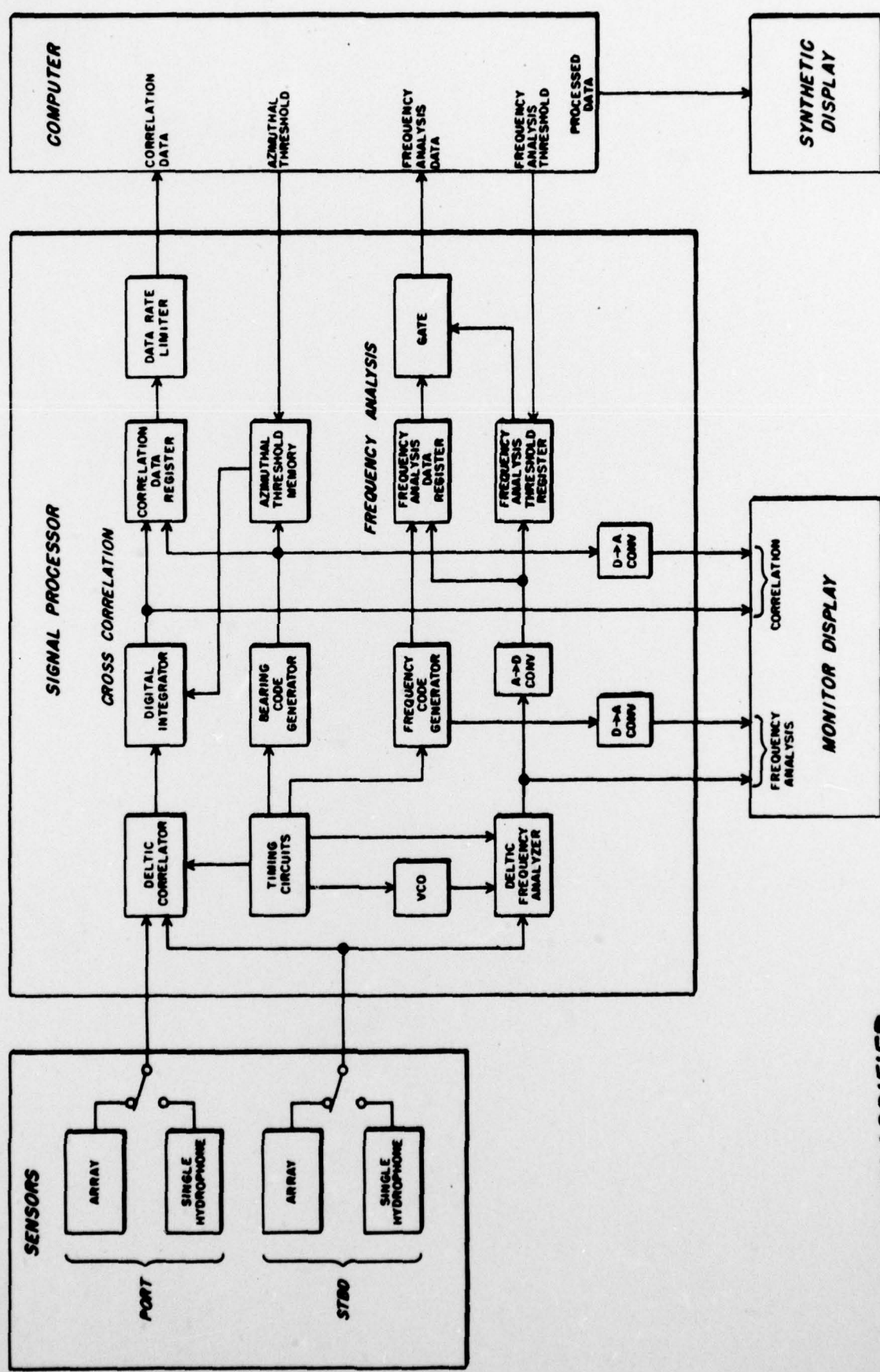


FIGURE 1 EXPERIMENTAL PASSIVE DETECTION SYSTEM

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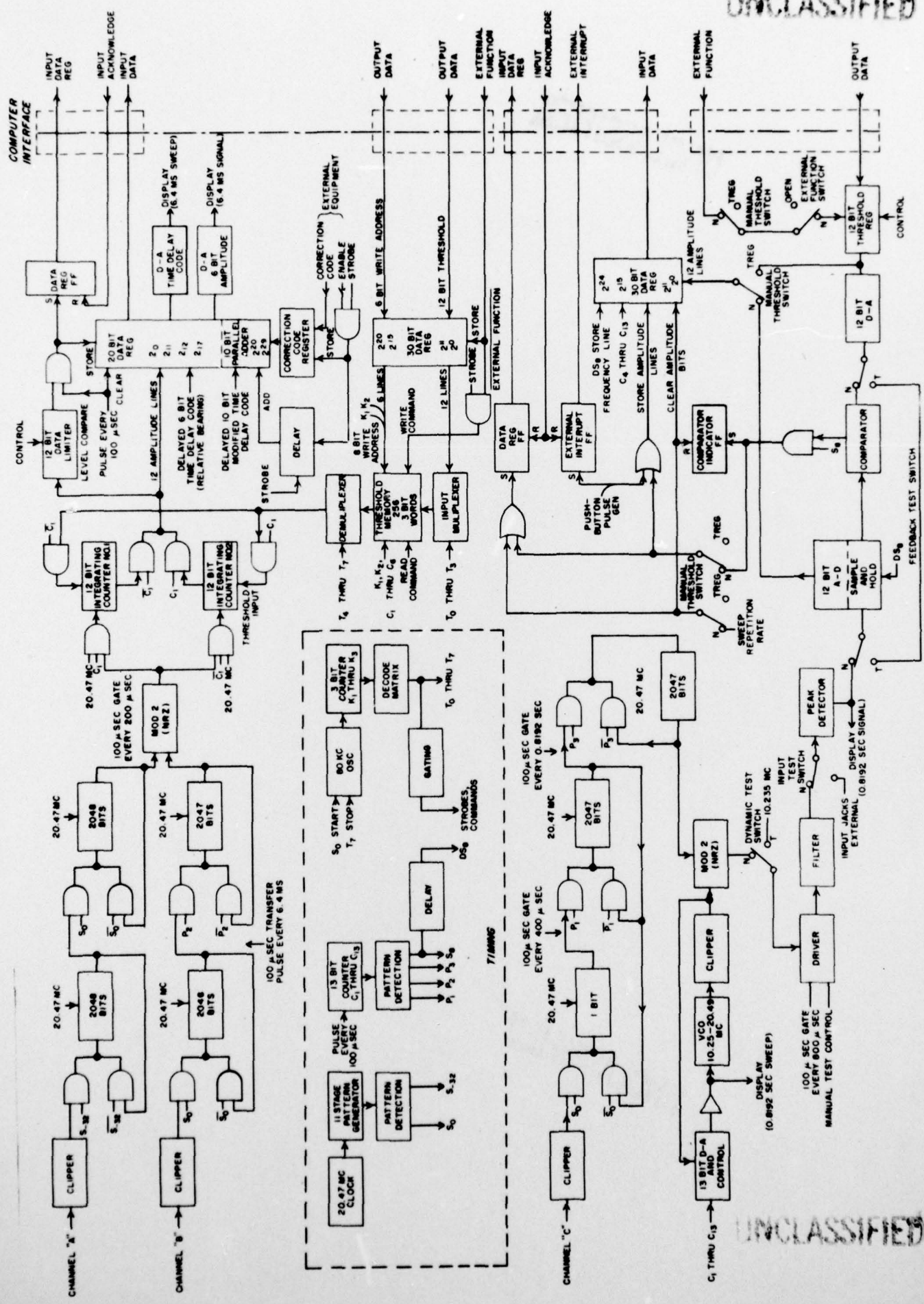


FIGURE 2 FUNCTIONAL BLOCK DIAGRAM  
DELTIC CROSS-CORRELATOR AND FREQUENCY ANALYZER

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